SCHOOL OF MECHANICAL & MATERIALS ENGINEERING

GRADUATE SEMINAR SERIES

Analysis of Corner Singularities and Cracks in Semiconductor Devices

Presented by

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Abstract

Modern semiconductor chips contain layers of alternating brittle dielectric materials and metal signal planes. The arrangement of these “Back-End-of Line” (BEOL) structures naturally introduces multi-material corners that are sources of high stress. In the drive towards improved performance, the dielectric materials are made more porous with every new technological node, exacerbating the stress concentration in BEOL structures. These brittle structures fracture when forces are transferred from the chip-substrate assembly or manufacturing process to the porous inter-layer dielectric structures. To ensure reliable BEOL structures, it is critical to understand the mechanistic causes of fracture, the potential crack initiation sites, and the ensuing crack path. In this talk, I will present computational modeling strategies as well as specialized computational tools for analyzing corner singularities, crack initiation and crack propagation in semiconductor devices. Specifically, I will demonstrate “load decomposition” as a modeling strategy to identify the mechanistic cause of fracture. I will present thermodynamic conditions on a moving interface (termed configurational-force) that provides a novel paradigm for integrating mechanics of fracture with thermodynamics. Such a thermodynamically consistent theory naturally generalizes and provides a unified criterion for crack initiation and propagation, unlike classical fracture mechanics. The theory is implemented in a large fracture analysis code and demonstrated to predict fracture in BEOL structures.

Biography

Ganesh Subbarayan is a Professor of Mechanical Engineering at Purdue University. He began his professional career at IBM Corporation (1990-1993). He holds a B.Tech degree in Mechanical Engineering (1985) from the Indian Institute of Technology, Madras and a Ph.D. (1991) in Mechanical Engineering from Cornell University. Dr. Subbarayan's core research is broadly concerned with developing computational techniques to seamlessly integrate CAD with CAE while practical aspects of his research are to model and experimentally characterize failure in microelectronic devices and assemblies. He was a pioneer in using geometric models directly for analysis, popularly referred to as Isogeometric Analysis. As an independent consultant, he contributed to ensuring reliable designs of Microsoft Kinect and Surface line of products. Among others, Dr. Subbarayan is a recipient of the 2005 Mechanics Award from the ASME EPP Division and the NSF CAREER award. He is a Fellow of ASME as well as IEEE, and he served as the Editor-in-Chief of IEEE Transactions on Advanced Packaging during 2002-2010. He also served as the topical editor for John Wiley’s Encyclopedia of Electrical and Electronics Engineering during 2011-2012.

Thursday, February 14, 2019
11:00am to Noon
ETRL room 101

Meet the speaker before the seminar in ETRL room 119, 10:30am to 10:50am. Light refreshments will be served.

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